PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-086407

(43)Date of publication of application : 31.03.1995

(51)Int.Cl. H01L 21/82
H01L 21/3205
H01L 27/04
H01L 21/822

(21)Application number : 05-224773

(22)Date of filing : 09.09.1993

(71)Applicant : FUJITSU LTD

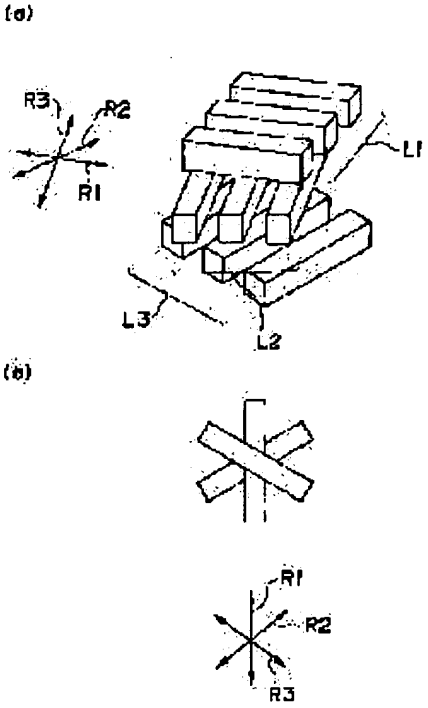
(72)Inventor : MIURA SHINPEI

(54) MULTILAYERED WIRING METHOD OF INTEGRATED CIRCUIT

(57)Abstract:

PURPOSE: To increase wiring efficiency of the layout of an integrated circuit, and provide a multilayered wiring method of an integrated circuit wherein wiring distance is short, by effectively using each wiring layer, in an integrated circuit wherein multilayered wiring is performed.

CONSTITUTION: In the multilayered wiring method of an integrated circuit wherein (m) kinds of wiring layers L1, L2 and L3 ((m) is three or larger positive integer) are formed, the main wiring directions of the (m) kinds of wiring layers L1, L2 and L are made different (n) kinds of wiring directions R1, R2 and R ((n) is positive integer satisfying 3≤≤m).



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] It is the multilayer-interconnection approach of the integrated circuit characterized by being n sorts (n being the positive integer of 3 <=n<=m) of wiring directions (R1, R2, and R3) where the wiring directions of Maine of said wiring layer (L1, L2, and L3) of m layers differ in the multilayer-interconnection approach of an integrated circuit equipped with the wiring layer (L1, L2, and L3) of m layers (m is three or more positive integers).
[Claim 2] Said n sorts of wiring directions (R1, R2, and R3) are the multilayer-interconnection approaches of the integrated circuit according to claim 1 characterized by crossing at include angles [each other].
[Claim 3] Said integrated circuit is the multilayer-interconnection approach of the integrated circuit according to claim 1 or 2 characterized by being integrated circuits equipped with a logic cell, such as a gate array and a standard cell.
[Claim 4] The multilayer-interconnection approach of said integrated circuit is the integrated-circuit multilayer-interconnection approach according to claim 3 characterized by considering that the terminal of said logic cell or said logic cell is a grid, and performing spacing between these grids using an equal isometrics trick grid.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the chip layout approach of an integrated circuit, in the integrated circuit which performs a multilayer interconnection especially, by using each wiring layer effectively, raised the wiring effectiveness in the layout of an integrated circuit, and relates to the multilayer-interconnection approach of the integrated circuit which can shorten wiring distance.
[0002] Multilayering of a wiring layer is progressing by large-scale-ization of the chip accompanying high integration in LSI in recent years. Therefore, it is necessary to make the efficient wiring technique accompanying multilayering of a wiring layer establish.
[0003]
[Description of the Prior Art] In the conventional semiconductor integrated circuit, the layout is performed by making into the Maine wiring direction the 2-way in every direction which crosses perpendicularly. The Maine wiring direction says the thing of the wiring direction fundamentally decided to each wiring layer here, and, as for the wiring direction of each wiring layer, it is completely common partially that wiring is made not in one direction but in the direction in which it differs (parts with which wiring is crowded).
[0004] For example, in three-layer wiring, as shown in drawing 5 (a) and (b), the wiring directions R11 and R12 where L12 [layer / 1st / layer / 2nd] intersects L11 perpendicularly were made into the wiring direction of Maine, and the wiring directions R12 and R11 where L13 [layer / 2nd / layer / 3rd] intersects L12 perpendicularly were further made into the wiring direction of Maine. As a result, the 3rd layer of the 1st layer of the direction where L13 is the same will be made into the wiring direction R11 of Maine with L11. In such a case, L12 [layer / 2nd] was used for fundamental wiring, and L13 [layer / 1st / layer / 3rd] was used auxiliary about L11 and a crowded part in many cases.
[0005]
[Problem(s) to be Solved by the Invention] Therefore, in the integrated circuit which performs the conventional multilayer interconnection, each wiring layer and especially wiring in the wiring layer after the 3rd layer did not use this wiring layer effectively, but had the problem that the wiring effectiveness of a layout was bad.
[0006] This invention aims at raising the wiring effectiveness in the layout of an integrated circuit, and offering the multilayer-interconnection approach of an integrated circuit with a short wiring distance by solving the above-mentioned trouble and using each wiring layer effectively in the integrated circuit which performs a multilayer interconnection.
[0007]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the multilayer-interconnection approach of the integrated circuit of the 1st description of this invention In the multilayer-interconnection approach of the integrated circuit equipped with the wiring layers L1, L2, and L3 of m layers (m is three or more positive integers) as shown in drawing 1 The wiring directions of Maine of said wiring layers L1, L2, and L3 of m layers are n sorts (n is the positive integer of 3

<=n<=m) of different wiring directions R1, R2, and R3.
[0008] Moreover, in said n sorts of wiring directions R1, R2, and R3, the multilayer-interconnection approach of the integrated circuit of the 2nd description of this invention crosses at include angles [each other] in the multilayer-interconnection approach of an integrated circuit according to claim 1.
[0009] Moreover, the multilayer-interconnection approaches of the integrated circuit of the 3rd description of this invention are integrated circuits with which said integrated circuit is equipped with a logic cell, such as a gate array and a standard cell, in the multilayer-interconnection approach of an integrated circuit according to claim 1 or 2.
[0010] Furthermore, the multilayer-interconnection approach of the integrated circuit of the 4th description of this invention considers that the terminal of said logic cell or said logic cell is a grid in the multilayer-interconnection approach of an integrated circuit according to claim 3, and the multilayer-interconnection approach of said integrated circuit is performed using an isometrics trick grid with equal spacing between these grids.
[0011]
[Function] By the multilayer-interconnection approach of the integrated circuit of the 1st and 2nd descriptions of this invention In the multilayer-interconnection approach of the integrated circuit equipped with the wiring layers L1, L2, and L3 of m layers (m is three or more positive integers, and is m= 3 at drawing 1) as shown in drawing 1 n sorts which are different in the wiring direction of Maine of said wiring layer of m layers, respectively (n is the positive integer of 3 <=n<=m) He considers as the wiring directions R1, R2, and R3 of n= 3, and is trying for n sorts of wiring directions R1, R2, and R3 to cross at include angles [each other] by the multilayer-interconnection approach of the integrated circuit of the 2nd description especially at drawing 1 .
[0012] Moreover, when referred to as m= 5 and n= 3, in an integrated circuit equipped with the wiring layers L1-L5 of five layers, it will wire the wiring direction of Maine of said wiring layer of m layers as three sorts of wiring directions R1, R2, R3, R1, and R2, respectively.
[0013] That is, in drawing 1 , by wiring using the wiring layers (the 1st, the 2nd, and the 3rd layer) L1, L2, and L3 of n layers which n sorts of wiring directions R1, R2, and R3 intersect at an equal include angle, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised. Moreover, since slanting wiring is attained, compared with the conventional wiring, the short layout of wiring distance is realizable.
[0014] Moreover, by the multilayer-interconnection approach of the integrated circuit of the 3rd and 4th descriptions of this invention, it considers that the terminal of a logic cell or a logic cell is a grid on the system which performs CAD of a layout to integrated circuits equipped with a logic cell, such as a gate array and a standard cell, and a wiring decision is made using an isometrics trick grid with equal spacing between these grids.
[0015] Thereby, while being able to attain automation of layout design, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised.
[0016]
[Example] Next, the example concerning this invention is explained based on a drawing.
The conceptual explanatory view of the multilayer-interconnection approach of the integrated circuit applied to the 1st example of this invention at 1st example drawing 1 is shown. Drawing 1 (a) is pictorial drawing and drawing 1 (b) is a top view. The integrated circuit of this example is wired using the wiring layer of three layers. As an integrated circuit, integrated circuits equipped with a logic cell, such as a gate array and a standard cell, are assumed.
[0017] this drawing -- setting -- L1 -- in the 2nd-layer wiring and L3, the Maine wiring direction of L1 and R2 express the wiring direction of L2, and, as for R3, the 3rd-layer wiring and R1 express [the 1st-layer wiring and L2] the 1st layer of the 2nd layer of the 3rd layer of the wiring direction of L3, respectively.
[0018] The multilayer-interconnection approach of the integrated circuit of this example considers that the terminal of a logic cell or a logic cell is a grid, and is performed using an isometrics trick grid with equal spacing between these grids. Drawing 2 (a) expresses the isometrics trick grid in this example. The

wiring directions R1, R2, and R3 of each class cross at include angles [each other] (60 [deg]).
[0019] Drawing 2 (b) shows the example of wiring in integrated circuits, such as a gate array and a standard cell. Among drawing, A is a logic cell and is 5 train preparation ****** about the cel train B which consists of 12 logic cells. Moreover, the 1st layer of the wiring direction R1 of L1 is perpendicular to a cel train.
[0020] In this drawing wiring between a node M1 and a node N1 wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- wiring L3- of the 3rd layer -- wiring L2- of the 2nd layer -- it wires with the 1st-layer wiring L1 -- having -- moreover, wiring between a node M2 and a node N2 -- wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- it wires with the 1st-layer wiring L1. Moreover, an about one node [N] isometrics trick grid and wiring are shown in this drawing (c).
[0021] thus, by the multilayer-interconnection approach of the integrated circuit by this example And the 3rd layer wires using L1, L2, and L3. the 1st which the wiring directions R1, R2, and R3 of each class intersect at an equal include angle, and the 2nd -- on a CAD system By using the structure model of an isometrics trick grid which considered that the terminal of a logic cell or a logic cell was a grid, and making a wiring decision, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised.
[0022] Moreover, in this example, since slanting wiring is attained, compared with the conventional wiring, the short layout of wiring distance is realizable.
The explanatory view of the multilayer-interconnection approach of the integrated circuit applied to the 2nd example of this invention at 2nd example drawing 3 is shown. Also in this example, it wires using the same (shown in drawing 1) wiring layer of three layers as the 1st example.
[0023] Drawing 3 (a) expresses the isometrics trick grid in this example. the 1st and the 2nd -- and the 3rd layer of the wiring directions R1, R2, and R3 of each class of L1, L2, and L3 crosses at include angles [each other] (60 [deg]).
[0024] Drawing 3 (b) shows the example of wiring in integrated circuits, such as a gate array and a standard cell. The 2nd layer of the wiring direction R2 of L2 is this direction to a cel train. this drawing -- setting -- wiring between a node M1 and a node N1 -- wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- it wires with the 3rd-layer wiring L3 -- having -- moreover, wiring between a node M2 and a node N2 -- wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- it wires with the 1st-layer wiring L1. Moreover, an about one node [N] isometrics trick grid and wiring are shown in this drawing (c).
[0025] Thus, also in the multilayer-interconnection approach of the integrated circuit by this example, the short layout of wiring distance is realizable from being able to use each wiring layer effectively, and being able to raise the wiring effectiveness in the layout of an integrated circuit, and slanting wiring being attained like the 1st example compared with the conventional wiring.
[0026] In addition, in the 1st and 2nd examples, the i-th layer, the directivity over the cel train of the wiring direction Ri of Li may not be limited to the above-mentioned contents, but may be what kind of combination.
The explanatory view of the multilayer-interconnection approach of the integrated circuit applied to the 3rd example of this invention at 3rd example drawing 4 is shown.
[0027] In this drawing, in R1, the wiring direction of L2 and R3 express the wiring direction of L3, and, as for R4, the Maine wiring direction of L1 and R2 express the 1st layer of the 2nd layer of the 3rd layer of the 4th layer of the wiring direction of L4, respectively.
[0028] The multilayer-interconnection approach of the integrated circuit of this example considers that the terminal of a logic cell or a logic cell is a grid, and is performed using the same square grid as usual. Drawing 4 (a) expresses the square grid in this example. The wiring directions R1, R2, R3, and R4 of each class cross at include angles [each other] (45 [deg]).
[0029] Drawing 4 (b) shows the example of wiring in integrated circuits, such as a gate array and a standard cell. Among drawing, A is a logic cell and is 5 train preparation ****** about the cel train B which consists of 12 logic cells. Moreover, the wiring direction R1 of L1 is perpendicular to a cel train, and the 2nd layer of the 1st layer of the wiring direction R2 of L2 is the same direction to a cel train.

[0030] In this drawing wiring between a node M1 and a node N1 It wires with the 1st-layer wiring L1. wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- wiring L4- of the 4th layer -- wiring L2- of the 2nd layer -- wiring between a node M2 and a node N2 wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- the 3rd -- wiring [of layer L3] - the 2nd -- wiring [of layer L2] - it wires with the 1st-layer wiring L1. Moreover, an about one node [N] isometrics trick grid and wiring are shown in this drawing (c).

[0031] thus, by the multilayer-interconnection approach of the integrated circuit by this example And the 4th layer wires using L1, L2, L3, and L4. the 1st which the wiring directions R1, R2, R3, and R4 of each class intersect at an equal include angle, the 2nd, and the 3rd -- on a CAD system By using the structure model of a square grid which considered that the terminal of a logic cell or a logic cell was a grid, and making a wiring decision, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised.

[0032] Moreover, in this example, since slanting wiring is attained, compared with the conventional wiring, the short layout of wiring distance is realizable.

[0033]

[Effect of the Invention] As explained above, according to this invention, it wires using the wiring layer of m layers which n sorts of wiring directions intersect at an equal include angle. On a CAD system Since a wiring decision is made using the structure model of a square grid which considered that the terminal of a logic cell or a logic cell was a grid Since each wiring layer can be used effectively, and the wiring effectiveness in the layout of an integrated circuit can be raised and slanting wiring is attained, The short layout of wiring distance can be realized compared with the conventional wiring, and the wiring effectiveness in the layout of an integrated circuit can be raised as a result, and the multilayer-interconnection approach of an integrated circuit with a short wiring distance can be offered.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] This invention relates to the chip layout approach of an integrated circuit, in the integrated circuit which performs a multilayer interconnection especially, by using each wiring layer effectively, raised the wiring effectiveness in the layout of an integrated circuit, and relates to the multilayer-interconnection approach of the integrated circuit which can shorten wiring distance.
[0002] Multilayering of a wiring layer is progressing by large-scale-ization of the chip accompanying high integration in LSI in recent years. Therefore, it is necessary to make the efficient wiring technique accompanying multilayering of a wiring layer establish.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] In the conventional semiconductor integrated circuit, the layout is performed by making into the Maine wiring direction the 2-way in every direction which crosses perpendicularly. The Maine wiring direction says the thing of the wiring direction fundamentally decided to each wiring layer here, and, as for the wiring direction of each wiring layer, it is completely common partially that wiring is made not in one direction but in the direction in which it differs (parts with which wiring is crowded).
[0004] For example, in three-layer wiring, as shown in drawing 5 (a) and (b), the wiring directions R11 and R12 where L12 [layer / 1st / layer / 2nd] intersects L11 perpendicularly were made into the wiring direction of Maine, and the wiring directions R12 and R11 where L13 [layer / 2nd / layer / 3rd] intersects L12 perpendicularly were further made into the wiring direction of Maine. As a result, the 3rd layer of the 1st layer of the direction where L13 is the same will be made into the wiring direction R11 of Maine with L11. In such a case, L12 [layer / 2nd] was used for fundamental wiring, and L13 [layer / 1st / layer / 3rd] was used auxiliary about L11 and a crowded part in many cases.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, it wires using the wiring layer of m layers which n sorts of wiring directions intersect at an equal include angle. On a CAD system Since a wiring decision is made using the structure model of a square grid which considered that the terminal of a logic cell or a logic cell was a grid Since each wiring layer can be used effectively, and the wiring effectiveness in the layout of an integrated circuit can be raised and slanting wiring is attained, The short layout of wiring distance can be realized compared with the conventional wiring, and the wiring effectiveness in the layout of an integrated circuit can be raised as a result, and the multilayer-interconnection approach of an integrated circuit with a short wiring distance can be offered.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Therefore, in the integrated circuit which performs the conventional multilayer interconnection, each wiring layer and especially wiring in the wiring layer after the 3rd layer did not use this wiring layer effectively, but had the problem that the wiring effectiveness of a layout was bad.
[0006] This invention aims at raising the wiring effectiveness in the layout of an integrated circuit, and offering the multilayer-interconnection approach of an integrated circuit with a short wiring distance by solving the above-mentioned trouble and using each wiring layer effectively in the integrated circuit which performs a multilayer interconnection.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the multilayer-interconnection approach of the integrated circuit of the 1st description of this invention In the multilayer-interconnection approach of the integrated circuit equipped with the wiring layers L1, L2, and L3 of m layers (m is three or more positive integers) as shown in drawing 1 The wiring directions of Maine of said wiring layers L1, L2, and L3 of m layers are n sorts (n is the positive integer of 3 <=n<=m) of different wiring directions R1, R2, and R3.
[0008] Moreover, in said n sorts of wiring directions R1, R2, and R3, the multilayer-interconnection approach of the integrated circuit of the 2nd description of this invention crosses at include angles [each other] in the multilayer-interconnection approach of an integrated circuit according to claim 1.
[0009] Moreover, the multilayer-interconnection approaches of the integrated circuit of the 3rd description of this invention are integrated circuits with which said integrated circuit is equipped with a logic cell, such as a gate array and a standard cell, in the multilayer-interconnection approach of an integrated circuit according to claim 1 or 2.
[0010] Furthermore, the multilayer-interconnection approach of the integrated circuit of the 4th description of this invention considers that the terminal of said logic cell or said logic cell is a grid in the multilayer-interconnection approach of an integrated circuit according to claim 3, and the multilayer-interconnection approach of said integrated circuit is performed using an isometrics trick grid with equal spacing between these grids.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

OPERATION

[Function] By the multilayer-interconnection approach of the integrated circuit of the 1st and 2nd descriptions of this invention In the multilayer-interconnection approach of the integrated circuit equipped with the wiring layers L1, L2, and L3 of m layers (m is three or more positive integers, and is m= 3 at drawing 1) as shown in drawing 1 n sorts which are different in the wiring direction of Maine of said wiring layer of m layers, respectively (n is the positive integer of 3 <=n<=m) He considers as the wiring directions R1, R2, and R3 of n= 3, and is trying for n sorts of wiring directions R1, R2, and R3 to cross at include angles [each other] by the multilayer-interconnection approach of the integrated circuit of the 2nd description especially at drawing 1 .
[0012] Moreover, when referred to as m= 5 and n= 3, in an integrated circuit equipped with the wiring layers L1-L5 of five layers, it will wire the wiring direction of Maine of said wiring layer of m layers as three sorts of wiring directions R1, R2, R3, R1, and R2, respectively.
[0013] That is, in drawing 1 , by wiring using the wiring layers (the 1st, the 2nd, and the 3rd layer) L1, L2, and L3 of n layers which n sorts of wiring directions R1, R2, and R3 intersect at an equal include angle, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised. Moreover, since slanting wiring is attained, compared with the conventional wiring, the short layout of wiring distance is realizable.
[0014] Moreover, by the multilayer-interconnection approach of the integrated circuit of the 3rd and 4th descriptions of this invention, it considers that the terminal of a logic cell or a logic cell is a grid on the system which performs CAD of a layout to integrated circuits equipped with a logic cell, such as a gate array and a standard cell, and a wiring decision is made using an isometrics trick grid with equal spacing between these grids.
[0015] Thereby, while being able to attain automation of layout design, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example] Next, the example concerning this invention is explained based on a drawing.
The conceptual explanatory view of the multilayer-interconnection approach of the integrated circuit applied to the 1st example of this invention at 1st example drawing 1 is shown. Drawing 1 (a) is pictorial drawing and drawing 1 (b) is a top view. The integrated circuit of this example is wired using the wiring layer of three layers. As an integrated circuit, integrated circuits equipped with a logic cell, such as a gate array and a standard cell, are assumed.
[0017] this drawing -- setting -- L1 -- in the 2nd-layer wiring and L3, the Maine wiring direction of L1 and R2 express the wiring direction of L2, and, as for R3, the 3rd-layer wiring and R1 express [the 1st-layer wiring and L2] the 1st layer of the 2nd layer of the 3rd layer of the wiring direction of L3, respectively.
[0018] The multilayer-interconnection approach of the integrated circuit of this example considers that the terminal of a logic cell or a logic cell is a grid, and is performed using an isometrics trick grid with equal spacing between these grids. Drawing 2 (a) expresses the isometrics trick grid in this example. The wiring directions R1, R2, and R3 of each class cross at include angles [each other] (60 [deg]).
[0019] Drawing 2 (b) shows the example of wiring in integrated circuits, such as a gate array and a standard cell. Among drawing, A is a logic cell and is 5 train preparation ****** about the cel train B which consists of 12 logic cells. Moreover, the 1st layer of the wiring direction R1 of L1 is perpendicular to a cel train.
[0020] In this drawing wiring between a node M1 and a node N1 wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- wiring L3- of the 3rd layer -- wiring L2- of the 2nd layer -- it wires with the 1st-layer wiring L1 -- having -- moreover, wiring between a node M2 and a node N2 -- wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- it wires with the 1st-layer wiring L1. Moreover, an about one node [N] isometrics trick grid and wiring are shown in this drawing (c).
[0021] thus, by the multilayer-interconnection approach of the integrated circuit by this example And the 3rd layer wires using L1, L2, and L3. the 1st which the wiring directions R1, R2, and R3 of each class intersect at an equal include angle, and the 2nd -- on a CAD system By using the structure model of an isometrics trick grid which considered that the terminal of a logic cell or a logic cell was a grid, and making a wiring decision, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised.
[0022] Moreover, in this example, since slanting wiring is attained, compared with the conventional wiring, the short layout of wiring distance is realizable.
The explanatory view of the multilayer-interconnection approach of the integrated circuit applied to the 2nd example of this invention at 2nd example drawing 3 is shown. Also in this example, it wires using the same (shown in drawing 1) wiring layer of three layers as the 1st example.
[0023] Drawing 3 (a) expresses the isometrics trick grid in this example. the 1st and the 2nd -- and the 3rd layer of the wiring directions R1, R2, and R3 of each class of L1, L2, and L3 crosses at include angles [each other] (60 [deg]).
[0024] Drawing 3 (b) shows the example of wiring in integrated circuits, such as a gate array and a

standard cell. The 2nd layer of the wiring direction R2 of L2 is this direction to a cel train. this drawing -- setting -- wiring between a node M1 and a node N1 -- wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- it wires with the 3rd-layer wiring L3 -- having -- moreover, wiring between a node M2 and a node N2 -- wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- it wires with the 1st-layer wiring L1. Moreover, an about one node [N] isometrics trick grid and wiring are shown in this drawing (c).

[0025] Thus, also in the multilayer-interconnection approach of the integrated circuit by this example, the short layout of wiring distance is realizable from being able to use each wiring layer effectively, and being able to raise the wiring effectiveness in the layout of an integrated circuit, and slanting wiring being attained like the 1st example compared with the conventional wiring.

[0026] In addition, in the 1st and 2nd examples, the i-th layer, the directivity over the cel train of the wiring direction Ri of Li may not be limited to the above-mentioned contents, but may be what kind of combination.

The explanatory view of the multilayer-interconnection approach of the integrated circuit applied to the 3rd example of this invention at 3rd example drawing 4 is shown.

[0027] In this drawing, in R1, the wiring direction of L2 and R3 express the wiring direction of L3, and, as for R4, the Maine wiring direction of L1 and R2 express the 1st layer of the 2nd layer of the 3rd layer of the 4th layer of the wiring direction of L4, respectively.

[0028] The multilayer-interconnection approach of the integrated circuit of this example considers that the terminal of a logic cell or a logic cell is a grid, and is performed using the same square grid as usual. Drawing 4 (a) expresses the square grid in this example. The wiring directions R1, R2, R3, and R4 of each class cross at include angles [each other] (45 [deg]).

[0029] Drawing 4 (b) shows the example of wiring in integrated circuits, such as a gate array and a standard cell. Among drawing, A is a logic cell and is 5 train preparation ****** about the cel train B which consists of 12 logic cells. Moreover, the wiring direction R1 of L1 is perpendicular to a cel train, and the 2nd layer of the 1st layer of the wiring direction R2 of L2 is the same direction to a cel train.

[0030] In this drawing wiring between a node M1 and a node N1 It wires with the 1st-layer wiring L1. wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- wiring L4- of the 4th layer -- wiring L2- of the 2nd layer -- wiring between a node M2 and a node N2 wiring L1- of the 1st layer -- wiring L2- of the 2nd layer -- the 3rd -- wiring [of layer L3] - the 2nd -- wiring [of layer L2] - it wires with the 1st-layer wiring L1. Moreover, an about one node [N] isometrics trick grid and wiring are shown in this drawing (c).

[0031] thus, by the multilayer-interconnection approach of the integrated circuit by this example And the 4th layer wires using L1, L2, L3, and L4. the 1st which the wiring directions R1, R2, R3, and R4 of each class intersect at an equal include angle, the 2nd, and the 3rd -- on a CAD system By using the structure model of a square grid which considered that the terminal of a logic cell or a logic cell was a grid, and making a wiring decision, each wiring layer can be used effectively and the wiring effectiveness in the layout of an integrated circuit can be raised.

[0032] Moreover, in this example, since slanting wiring is attained, compared with the conventional wiring, the short layout of wiring distance is realizable.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the conceptual explanatory view of the multilayer-interconnection approach of the integrated circuit concerning the 1st example of this invention, and drawing 1 (a) is pictorial drawing and drawing 1 (b) is a top view.
[Drawing 2] It is the explanatory view of the multilayer-interconnection approach of the integrated circuit of the 1st example, and the example [in / drawing 2 (a), and / in drawing 2 (b) / integrated circuits, such as a gate array and a standard cell,] of wiring and drawing 2 (c) are explanatory views about an about one node [N] isometrics trick grid and wiring. [the explanatory view of an isometrics trick grid]
[Drawing 3] It is the explanatory view of the multilayer-interconnection approach of the integrated circuit of the 2nd example of this invention, and the example [in / drawing 3 (a), and / in drawing 3 (b) / an integrated circuit] of wiring and drawing 3 (c) are explanatory views about an about one node [N] isometrics trick grid and wiring. [the explanatory view of an isometrics trick grid]
[Drawing 4] It is the explanatory view of the multilayer-interconnection approach of the integrated circuit of the 3rd example of this invention, and the example [in / drawing 4 (a), and / in drawing 4 (b) / an integrated circuit] of wiring and drawing 4 (c) are explanatory views about an about one node [N] isometrics trick grid and wiring. [the explanatory view of a square grid]
[Drawing 5] It is the conceptual explanatory view of the multilayer-interconnection approach of the conventional integrated circuit, and drawing 5 (a) is pictorial drawing and drawing 5 (b) is a top view.
[Description of Notations]
L1, L2, L3, L4 -- The 1st, the 2nd, the 3rd, and the 4th layer (wiring of an eye)
R1, R2, R3, R4 -- The 1st, the 2nd, the 3rd, and the wiring direction of the 4th layer
A -- Logic cell
B -- Cel train
M1, M2, N1, N2 -- Node

[Translation done.]

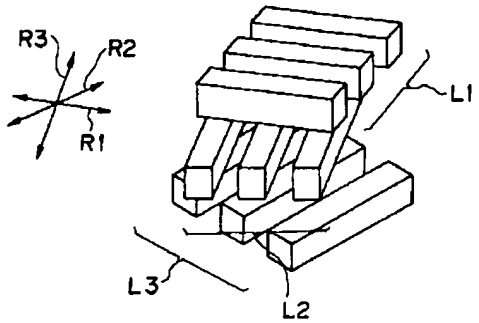
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

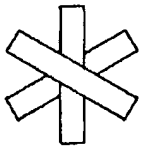
DRAWINGS

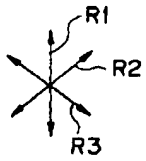
[Drawing 1]
第1実施例の集積回路の配線方法の概念説明図

(a) 立体図



(b) 平面図

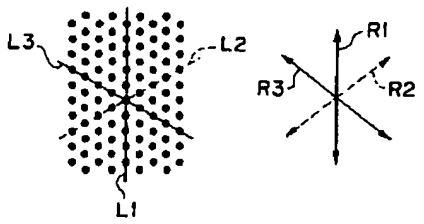




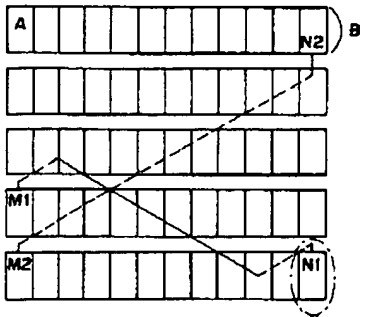
[Drawing 2]

第１実施例の集積回路の配線方法の説明図

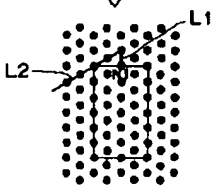
(a) アイソメトリック・グリッド



(b) 集積回路における配線例



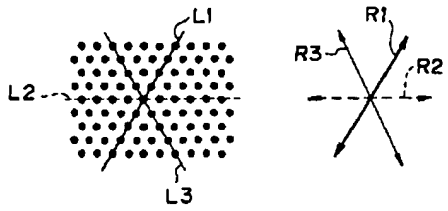
(c) ノードN1近傍のグリッド及び配線



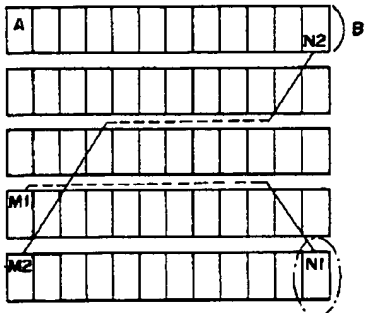
[Drawing 3]

第２実施例の集積回路の配線方法の説明図

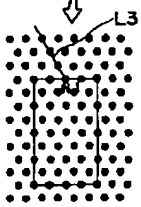
(a) アイソメトリック・グリッド



(b) 集積回路における配線例



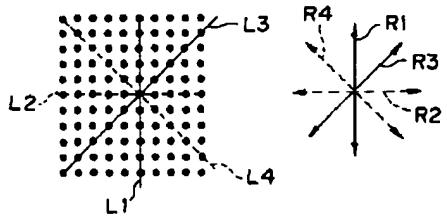
(c) ノードN1近傍の
グリッド及び配線



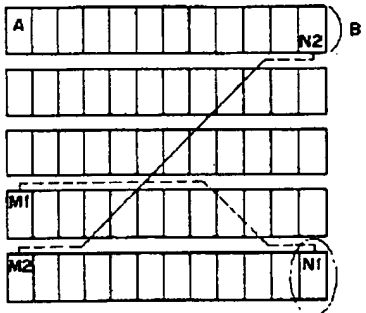
[Drawing 4]

第３実施例の集積回路の配線方法の説明図

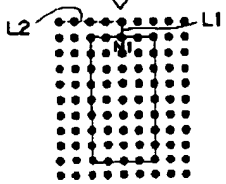
(a) 平方グリッド



(b) 集積回路における配線例



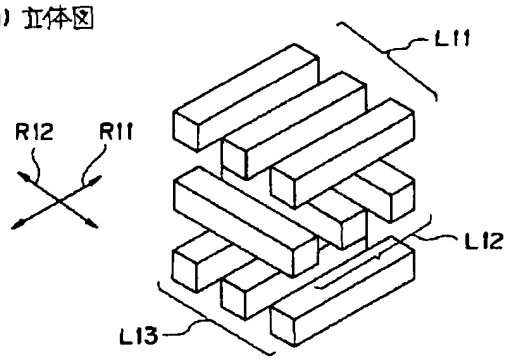
(c) ノードN1近傍のグリッド及び配線



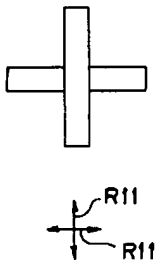
[Drawing 5]

従来の多層配線の説明図

(a) 立体図



(b) 平面図



[Translation done.]